

## Transmitter Pre-emphasis and Adaptive Receiver Equalization for Duobinary Signaling in Backplane Channels

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**Abstract.- In this paper, an adaptive equalization technique of a multi-gigabit channel using duobinary signaling is proposed. Both the receiver and transmitter are equalized and implemented using ADS. The results show that the duobinary signaling performs better than NRZ at half of the bandwidth. The algorithm was tested in a Tyco XAUI-FR4 backplane.**

### 1. INTRODUCTION

At low frequencies, transmission media (PCB traces, packages, etc) has little effect on signals. However, as clock frequency increases, the transmission media exhibits capacitive and inductive characteristics, therefore, adversely affecting signal integrity. On the other hand, consumer electronics applications such as 3D graphics, wireless communications, and high definition video, demand a huge bandwidth at the board level, which in turn pushes the bandwidth of the chips and PCBs used to their limits. Therefore, data rate of chip-to-chip communication on PCBs is not only limited by the clock speed of the transceiver, but also by the bandwidth of the transmission media. To increase data rate to 5 GB/s and higher, equalization and Multi-Level Signaling (MLS) are being researched [1-10]. In systems with equalization, pre-emphasis, based on FIR filters, is performed to boost high frequency signal content on the transmitter side and decision feedback equalization, along with linear feed-forward equalization, is used to combat reflections at the receiver [2]. The FIR pre-emphasis and receiver filters coefficients are first optimized using the LMS algorithm [11]; then, the updated coefficients are communicated back to the far-end transmitter where they are applied. These coefficients are continuously updated, to allow for correction of the impairments of the packages, connectors, and backplane traces; and other problems such as power-supply drift, component aging, and temperature variations [3]. In [1], Zerbe *et. al.* proposed a new equalization and clock recovery scheme for a 2.5-10-Gb/s 2-PAM/4-PAM backplane transceiver cell. This solution provided good performance at the cost of increased system complexity and power consumption. As described in [1], 4-PAM is a MLS scheme, which has four voltage levels and three decision thresholds. In 4-PAM, two binary bits are coded as one symbol; in other words, the baud rate of 4-PAM is half that of NRZ signaling. Unfortunately, 4-PAM signaling results in increased sensitivity to crosstalk and/or reflection as well as increased system complexity. In 4-PAM, the increased system complexity was mainly due to the clock data recovery (CDR) circuit at the receiver [1]. Also, the higher levels in 4-PAM increases the power

consumption in the circuitry involved. With MLS, signal-to-noise ratio (SNR) is sacrificed in exchange for a narrow bandwidth requirement. In [9], Sinsky proposed a three level signaling scheme called duobinary signaling, which performed better than 4-PAM. Duobinary signaling is a scheme in which  $R$  bits/sec are transmitted with less than  $R/2$  Hz of bandwidth; where,  $R/2$  Hz is the Nyquist rate for transmission without any Inter Symbol Interference (ISI). Duobinary is a type of partial-response signaling (PRS) [6]. The controlled amount of ISI is used to shape the spectrum of transmission channel, for instance, to place nulls in the frequency response. Also, this makes the receiver less sensitive to timing errors. The design in [9] consisted of three main blocks for implementing duobinary signaling, namely, precoder circuit, transmitter FIR filter and duobinary-to-binary converter. The design implemented the transmitter filter using D flip-flops and an attenuator. It was a simple filter whose coefficients are fixed for every channel. The research concluded that backplane duobinary signaling was still in experimental state and that adaptive equalization and inbuilt error correcting capabilities of duobinary signaling was not explored in [9].

This paper aims to achieve better signal quality (SNR) at a data rate higher than the data rate in [7, 9], by designing a receiver equalizer. Another goal in this paper is to employ adaptive equalization to combat temperature and parameter variations. The data rate achieved in [9] is 10 GB/s for 34" long trace backplanes; therefore, the design in this paper is geared towards achieving a better data rate (20 GB/s) than [9] and open the output eye at the same data rate. As discussed in the preceding sections, there was no adaptive equalization employed in [9]. However, we need adaptive equalization to combat the variations in the channel. For example, the channel scattering (S)-parameter varies mainly due to temperature changes, which in turn cause variations in dielectric loss. In this paper, the fixed transmitter filter in Sinsky's design is replaced by an adaptive transmitter FIR filter. Also, an adaptive receiver filter is used along with a transmitter filter to shape the duobinary signals according to the channel conditions. The filter coefficients are obtained using the LMS convergence algorithm. The design is formulated keeping in mind two goals: (i) efficient equalizer and (ii) simple architecture, for example, minimum number of taps. Differential S-parameters were generated from single ended S-parameters using the measurement equation along with the S-parameter simulation tool in ADS. Data

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Access component (DAC) in ADS was used to create a two-port network with differential S parameters [12] (Fig. 1)

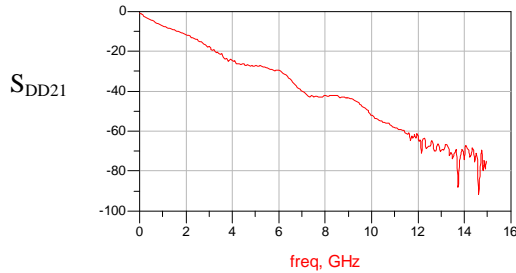


Fig. 1 Insertion Loss SDD21

## 2. RESULTS OF DUOBINARY SIGNALING

Fig. 2 shows the proposed architecture. Data was generated by a PRBS source and was sent through the precoder circuit to avoid continuous sequence of ones and zeros. To demonstrate the performance of the system Fig. 3 shows the channel output without equalization. The transmitter used a two-tap filter. After passing through the channel, the pre-distorted filter output (Fig. 4) is changed into duobinary waveform. The output of the channel is again sent through three tap receiver equalizers to improve the eye quality. The coefficients of the receiver filter were obtained using the LMS algorithm in ADS. The resulting eye diagrams are shown in figure 5 and 6. The vertical and horizontal eye opening for NRZ waveform was 0.15 V and 35 ps, respectively. The duobinary eye with half the bandwidth has vertical and horizontal eye opening of 0.24 V and 60 ps. Thus, duobinary signaling is more immune to timing jitter than NRZ. (Note all vertical axis in Figs. 3 to 6 are voltage levels)

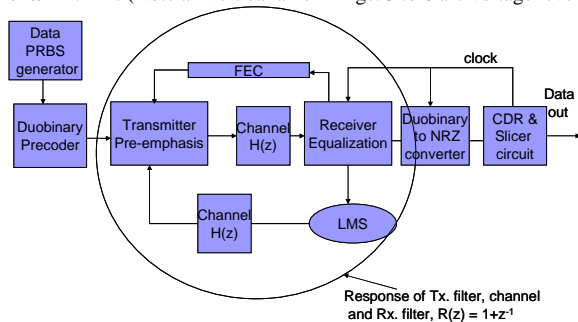


Fig. 2: Proposed Architecture

## 3. CONCLUSIONS

Using duobinary signaling accomplishes two tasks: reduction of the bandwidth and simplification of the architecture design in [4]. The use of transmitter and receiver equalizers achieves better quality at greater data rate than [2]. Additionally, the error correcting capabilities of duobinary signaling could be exploited. The NRZ signaling scheme with transmitter pre-emphasis was developed for a basis of comparison between the NRZ and duobinary scheme. Initial results show that duobinary performs better than NRZ.

## 4. REFERENCES

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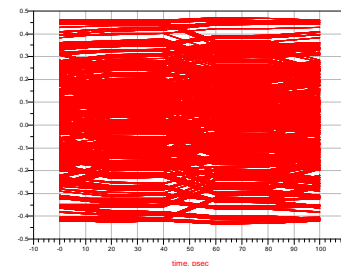


Fig. 3: Channel Output without any Equalization

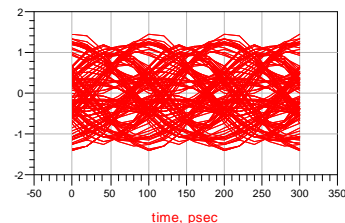


Fig. 4: Eye at the channel input

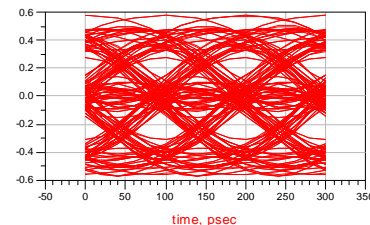


Fig. 5: Eye at the channel output

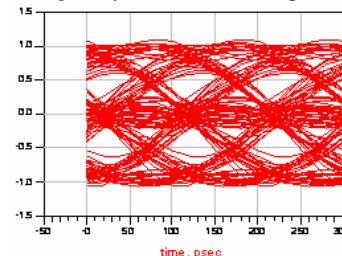


Fig. 6: Eye after receiver equalization.