

Characterization of Differential Via Holes Using Equivalent Circuit Extraction Technique

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ABSTRACT: A fast and accurate characterization method of differential via holes is presented based on the equivalent circuit extraction technique. A 3-D model of differential via holes is created and simulated using a full wave solver and the results are compared with the equivalent circuit model using Advanced Design System software. Results presented validate the proposed approach. © 2007 Wiley Periodicals, Inc. *Int J RF and Microwave CAE* 00: 000–000, 2007.

Keywords: differential via; circuit extraction; characterization

I. INTRODUCTION

Via holes are used to connect traces residing on different layers of a printed circuit board (PCB). Depending upon the geometric structure and placement inside the board, via holes are classified as single, differential, blind, or buried. A single via hole is a vertical connection through the board that could extend from the top layer to the bottom layer. Similarly, a differential via hole comprises a pair of via holes, which connect layers in a PCB board. A blind via hole is a vertical structure that stretches from the external layer to an internal layer without passing through the entire vertical stack-up layer. A buried via hole is a vertical structure that is placed between internal layers without passing through the entire vertical stack-up layers.

Pairs of via holes, using differential signaling, have become popular choices for high-speed digital transmission on a PCB. They offer superior immunity to crosstalk and external noise, and increase transmission bandwidth. However, the discontinuities intro-

duced by via holes are well-known impedance disruptors at high speeds in a PCB. Therefore, researchers have been studying different characterization methods for differential vias to improve their performance.

In [1, 2], Laermans et al. used a characterization method to model differential via holes as a cascade of capacitances and inductances. This method used special software, FASTCAP [3], to calculate the values of the capacitances and inductances at each designated location on via holes, and therefore calculate impedances at those points. Chen et al. [4] analyzed a large number of vias and differential signaling in multilayered structures using the equivalence principle, where a vertical via structure was decomposed into an interior and an exterior problem. In [5], full-wave modeling for differential signaling was used to extract a differential SPICE via model. The drawback is that these methods are time-consuming. Alternatively, in [6, 7], Antonini et al. used an equivalent circuit extraction technique approach for characterization of a single via hole in a PCB. Their approach, however, was only used for characterization of a single via hole and not for differential via holes. This article extends the equivalent circuit extraction technique, described in [6, 7], for differential via holes characterization on a PCB, in a fast and accurate manner.

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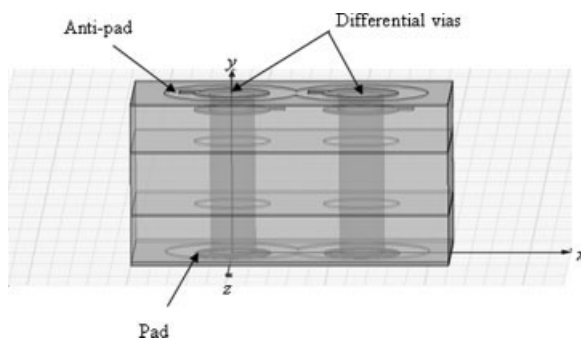


Figure 1. An example of a differential via hole structure in a multilayered environment.

This approach can be briefly described as follows: a differential via hole structure in a multilayered PCB is partitioned into three elementary structures, namely the top, the intermediate, and the bottom structures. An equivalent circuit is extracted from each partition and the scattering (S) parameters of each equivalent circuit are obtained. Then, a complete equivalent circuit for the entire differential via geometry is constructed by cascading all of the elementary equivalent circuit structures using Advanced Design System (ADS) software. To validate the approach used here, the S -parameters of this circuit are compared with those obtained from High Frequency Simulation Software (HFSS) and the measured S -parameters results are presented in [1, 4]. This article is organized as follows: in Section 2, via holes are briefly reviewed. The extraction technique of the equivalent circuit for each elementary structure is discussed in Section 3. In Section 4, the via and equivalent circuit parameters are calculated. In Section 5, S -parameters results from ADS, HFSS, and the equivalent circuit are compared. Conclusions are given in Section 6.

II. VIA HOLES REVIEW

Via holes in a multilayered PCB are used to connect signal traces from the top layer to intermediate layers and/or the bottom layer, or between intermediate layers. Because of the discontinuities introduced by via holes along the transmission path, there is some incident wave energy that reflects back to the source. The amount of the reflection depends upon the mismatch impedance between the source characteristic impedance and the transmission path impedance. A single via hole consists of a central cylinder, as well as numbers of thin, cylindrical, copper pads. Vias are passed through a number of copper ground planes by means of clearance holes (anti-pads). The entire geo-

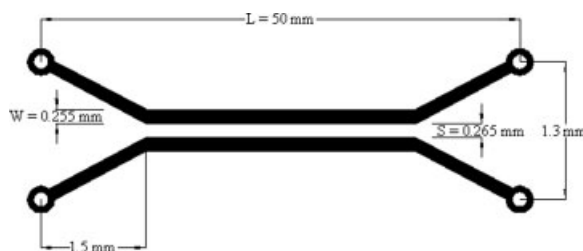


Figure 2. Top view of complete structure under study.

metrical structure is embedded into a dielectric material, usually FR-4. Differential via holes consist of two via holes, where the signal is sent differentially through a pair of strip-lines. Based upon the properties of a PCB geometrical structure (its trace lengths, widths, separations, and its thickness), differential via holes are designed to minimize the reflection and the attenuation of the signal. An example of differential via holes structure is shown in Figure 1.

III. EQUIVALENT CIRCUIT EXTRACTION TECHNIQUE FOR DIFFERENTIAL VIA HOLES

In [6, 7], the procedure for extracting the equivalent circuit of a via hole in a multilayered PCB is done as follows; a via hole is partitioned in three elementary structures: one for the top layer, one for the intermediate layer(s), and the last one for the bottom layer. Then, an equivalent circuit is obtained in the form of a two-port network for each elementary structure, where the elements of this two-port network depend on the via resistance (R_{via}), inductance (L_{via}), and capacitance (C_{via}); pad capacitance (C_{pad}), and interplanes capacitance (C_{ip}) values. These parameter values are calculated using formulas found in [7]. Next, a complete two-port network, representing the complete equivalent circuit of the via structure, is

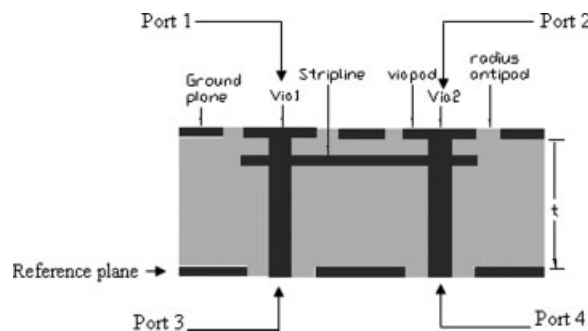


Figure 3. Top layer elementary structure.

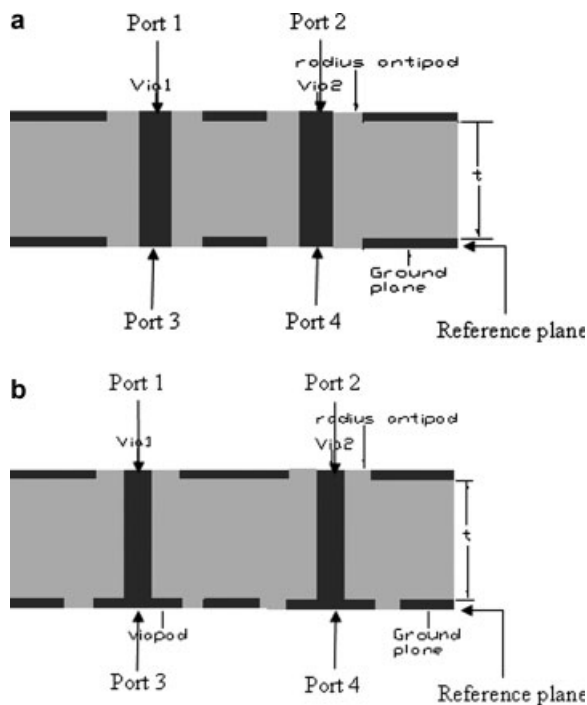


Figure 4. (a) Elementary structure for the intermediate layer; (b) Elementary structure for the bottom layer.

obtained by cascading each two-port network of every elementary equivalent circuit from the top to the bottom layer.

In this work, we extend the above technique to differential via pairs. The top view of the differential via structure under study here is shown Figure 2, and it is divided in three elementary structures: top, (Fig. 3), intermediate (Fig. 4a), and bottom layers (Fig. 4b).

As shown in Figure 3, an edge-coupled stripline connects via 1 and via 2 in the top layer elementary structure. The differential signal enters the structure at the port 1, travels through the stripline, and then

exits from the port 2. The characteristic impedance Z_0 of the edge-couple stripline is defined in [8]

$$Z_0 = \frac{80}{\sqrt{\epsilon_r}} \ln \left(\frac{1.9(2B + T)}{0.8W + T} \right) \left(1 - \frac{B}{4H} \right)$$

$$H > B, 0.1 < \frac{W}{B} < 2.0, \frac{T}{B} < 0.25, 1 < \epsilon_r < 15$$

where Z_0 is the characteristic impedance of the strip-line (Ω); ϵ_r is the relative dielectric constant; H is the height of the substrate FR4 under the stripline; B is the height of the substrate FR4 above the stripline; T is the thickness of the trace; W is the trace width.

We used SCLIN model in ADS to represent the edge-coupled stripline. The length (L) of stripline is 50 mm. The spacing (S) between stripline is 0.265 mm. The width (W) of stripline is 0.255 mm. The substrate material is FR4, which has a relative dielectric permittivity ϵ_r of 4.0.

Each elementary structure in the differential pair is modeled as serial interconnection of two two-port networks, one for each via of the differential pair. For example, the complete equivalent circuit for the top layer is shown in Figure 5.

The top portion of the equivalent circuit shown in Figure 5 represents the equivalent circuit of one via hole, and the bottom portion represents the equivalent circuit of the other via hole, which physically correspond to the via-pair shown in the left hand side of Figure 2 and the side view of the left hand side of Figure 3. Both parts are connected as series two-port network to form the equivalent circuit of the top layer differential via hole structure. Note that one advantage of using a two-port network is that if the impedance parameters are known, the behavior of two-port network can be modeled as an equivalent circuit. For instance, the impedance (Z) of the equivalent circuit

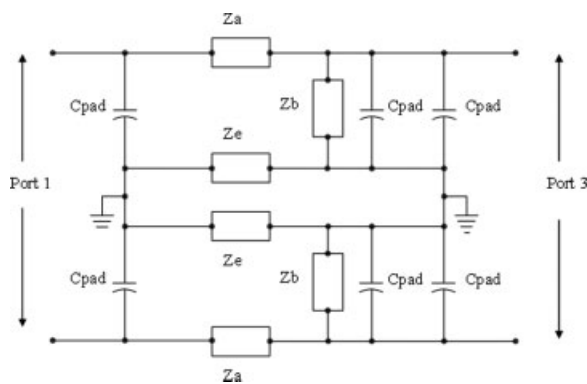


Figure 5. Equivalent circuit for the top layer structure.

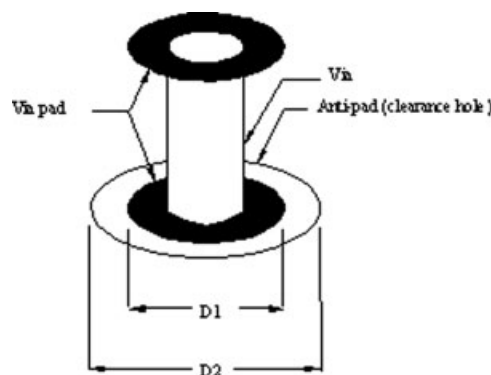


Figure 6. Typical via structure.

TABLE I. Calculated RLC Parameters of Via Structures

Via Parameters	Top Layer	Intermediate Layer	Bottom Layer
Resistance (R_{via})	0.015 Ω	0.015 Ω	0.015 Ω
Inductance (L_{via})	3.095pH	5.378pH	3.095pH
Capacitance (C_{via})	24.64fF	32.3fF	24.64fF
Interplane capacitance (C_{ip})	58.64pF	44.72pF	58.64pF

two-port network, shown in Figure 5, can be expressed in matrix form as:

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$$

where $Z_{11} = (Z_a Z_b + Z_b^2 + Z_b Z_e) / (Z_a + 2Z_b + Z_e)$ is the open-circuit input impedance, $Z_{12} = Z_{21} = (Z_b^2) / (Z_a + 2Z_b + Z_e)$ are the open-circuit transfer impedances, and $Z_{22} = (Z_a Z_b + Z_b^2 + Z_b Z_e) / (Z_a + 2Z_b + Z_e)$ is the open-circuit output impedance.

Note that each element of the impedance matrix entry can be determined by substituting for Z_a , Z_b , and Z_e , where $Z_a = R_{\text{via}} + j\omega L_{\text{via}}$, $Z_b = 1 / (j\omega C_{\text{via}})$, and $Z_e = 1 / (j\omega C_{\text{ip}})$. The second C_{pad} in the right hand side of Figure 5 is due to the stripline connection to the via (see also Figs. 1 and 3). These impedances along with C_{pad} parameter will be defined in the next section. Similar impedance calculations are applied to the elementary structures of the intermediate and bottom layers, which are shown in Figures 4a and 4b.

IV. VIA AND EQUIVALENT CIRCUIT PARAMETER CALCULATION

In this section, we discuss the via geometry that will drive its parameter calculation (R_{via} , C_{via} , L_{via} , etc.), which in turn will be used to obtain the equivalent

circuit impedances of each elementary two-port network. The final equivalent circuit is obtained by cascading each two-port network.

The stripline shown in the top layer structure, depicted in Figure 3, was modeled in ADS as an edge-coupled stripline (SCLIN). The followings are the parameters of this SCLIN: the substrate material is FR4, which has a relative dielectric permittivity ϵ_r of 4.0, and a loss tangent of 0.015 as described in [1]. In addition, the stripline model has conductivity per unit length of 5.8×10^7 S/m [1]. The trace width (W), thickness (T), spacing (S), and length (L) are 0.255 mm, 0.03 mm, 0.265 mm, and 50.0 mm, respectively.

For each via in the top layer, one of the most important parameters is the parasitic capacitance from the via pad to ground. This capacitance (in pF) is defined in [9] as:

$$C_{\text{pad}} = \frac{(1.41)\epsilon_r T D_1}{(D_2 - D_1)}$$

where D_1 is the diameter of via pad (2.992×10^{-2} in. ≈ 0.759968 mm), D_2 is the diameter of anti-pad (5.354×10^{-2} in. ≈ 1.359916 mm), as shown in Figure 6, T is the thickness of dielectric material, and ϵ_r was defined earlier.

Another important via parameter is the shunt capacitances, which are measured from the via to a ground plane. The amount of capacitance (C_{via}) depends upon the distance between the radius of the via and the radius of the anti-pad. In general, the following rule of thumb applies: the shorter the distance the higher the shunt capacitance. The shunt capacitances contribute to the trace impedance, and thus cause reflections. In addition, other important via parameter is the interplane capacitances (C_{ip}), which are measured between two ground planes. The amount of capacitance depends upon the physical geometry of the ground plane, as well as the thickness of the dielectric material. These via capacitances are calculated using equations found in [7].

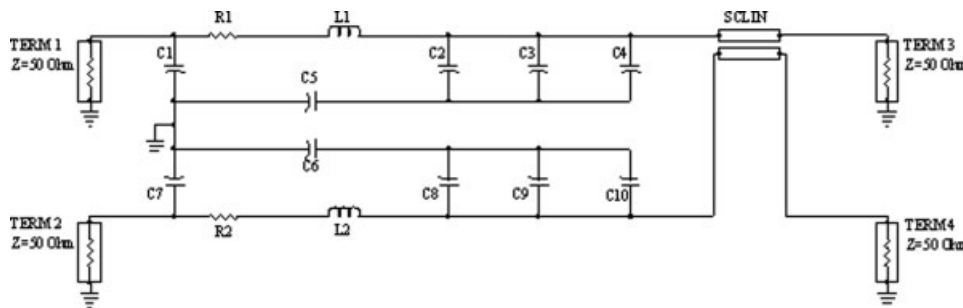


Figure 7. Actual equivalent circuit of the top layer, including stripline, built in ADS.

TABLE II. RLC Values of Actual Equivalent Circuit of the Top Layer

	Figure	Values
Resistance (R_1, R_2)	7	0.015Ω
Inductance (L_1, L_2)	7	3.095pH
Capacitance C_{pad} ($C_1, C_3, C_4, C_7, C_9, C_{10}$)	7	0.2124pF
Capacitance C_{via} (C_2, C_8)	7	24.64fF
Capacitance C_{ip} (C_5, C_6)	7	58.64pF
SCLIN	7	$W = 0.255\text{mm}$ $S = 0.265\text{mm}$ $L = 50\text{mm}$
Term (1, 2, 3, 4)	7	$Z = 50\Omega$

In addition, digital designers have considered the via inductance to be more crucial than the capacitance itself. Every via is known to have a parasitic series inductance (L_{via}), this is due to the physical structure of the via being too small, thus the behavior of via is very much like lump circuit elements. The primary effect of the series via inductance is that it degrades the signal that travels through the via, and decreases the effective decoupling capacitance. The inductance of the signal via depends upon the location of the return path associated with the signal via. Via inductance is also calculated using equations found in [7].

In high-speed applications, via and trace resistances are the combination of DC and AC resistances, where the AC resistance is due to the skin effect [10]. The total resistance is defined in [10] as follows:

$$R_{\text{Total}}(f) = \sqrt{R_{\text{DC}}^2 + R_{\text{AC}}^2(f)}$$

where the AC resistance is proportional to the square root of the frequency [10]. It is important to point out that the skin effect is already incorpo-

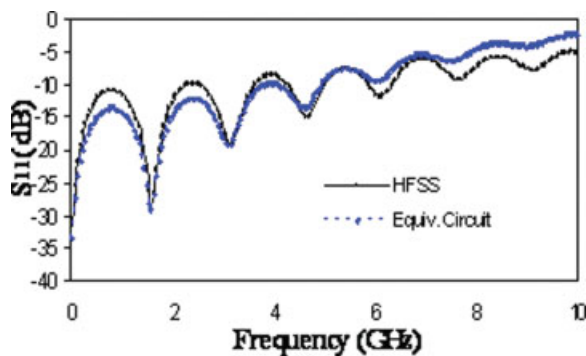


Figure 8. HFSS versus equivalent circuit simulation S_{11} parameter for the top layer structure. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

rated into the ADS software; therefore, accounting for DC and AC resistances due to all frequencies of interest.

The via parameter definitions described above were used to calculate the elements of the two-port network equivalent circuit used for the top layer, shown in Figure 5. The impedance $Z_a = R_{\text{via}} + j\omega L_{\text{via}}$ is associated with the total resistance and inductance of the via, $Z_b = 1/(j\omega C_{\text{via}})$ is the impedance associated with the via capacitance, and $Z_e = 1/(j\omega C_{\text{ip}})$ is the impedance between two ground planes. As mentioned, the top portion of the equivalent circuit shown in Figure 5 represents the equivalent circuit of one via hole, and the bottom portion represents the equivalent circuit of the other via hole.

The two-port network equivalent circuits for the intermediate and bottom layers are similar to the top layer circuit shown in Figure 5, with proper adjustments for via capacitance, inductance, and resistance. The calculated values of via resistances, inductances, capacitances, and interplane capacitances for the top layer, the intermediate layer, and the bottom layer are shown in Table I. Note that Columns 1 and 3 are the same; this may not be necessarily true for other geometries. The total structure including top, intermediate, and bottom layers as well as the stripline is shown in Figure 10.

The obtained equivalent circuit network for each layer is simulated in ADS and its S -parameters S_{11} (reflection coefficient) and S_{21} (the transmission coefficient) are found. These S -parameters are compared with those obtained from the corresponding differential via structure using HFSS. Next, a complete equivalent circuit network is obtained by cascading each two-port network equivalent circuit from the top to the bottom layer, and then the

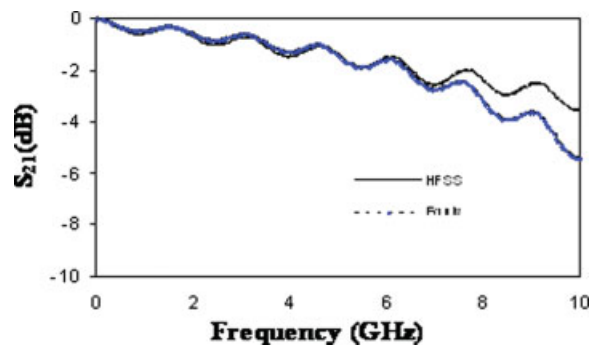


Figure 9. HFSS versus equivalent circuit simulation S_{21} parameter for the top layer structure. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

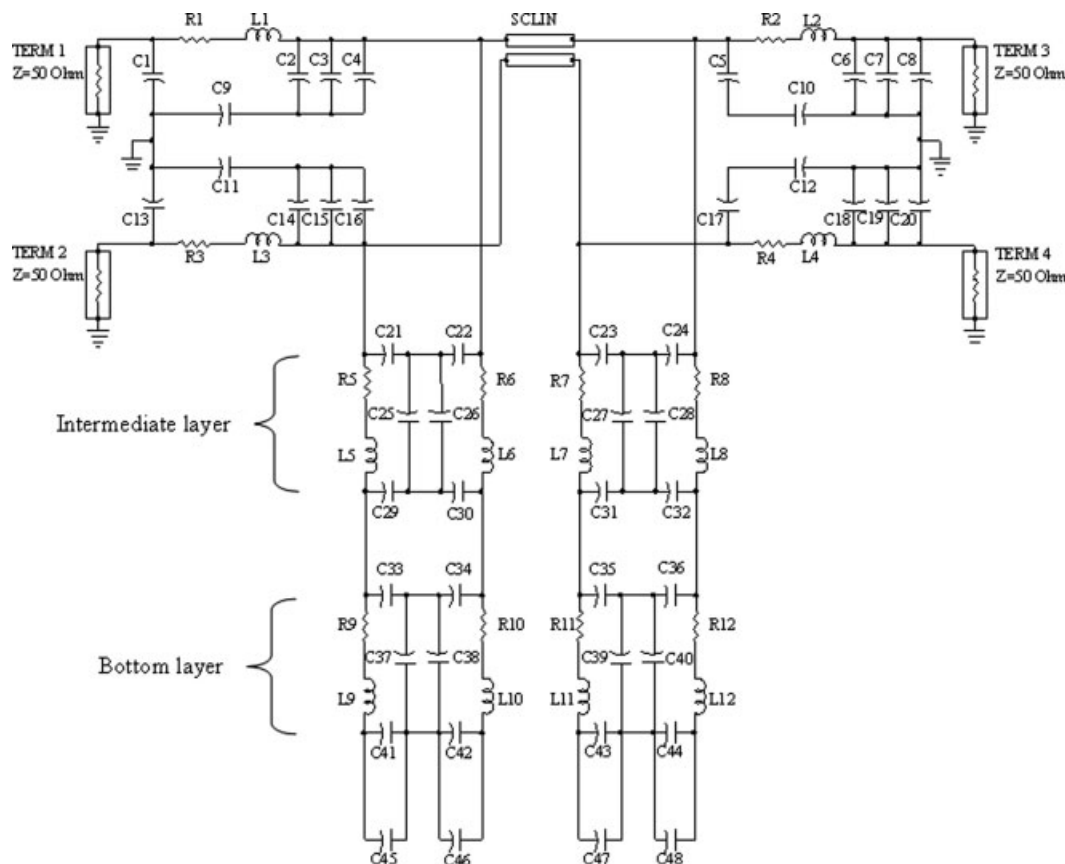


Figure 10. Equivalent circuit model of the complete structure.

S-parameters S_{11} and S_{21} are determined from ADS. The S-parameters of the complete differential via structure are also compared with those obtained from the same differential via structure using HFSS. All the S-parameters were evaluated from 50 MHz to 10 GHz. In the following section, results will be presented, which will validate the derived equivalent

circuit for each of the elementary and complete differential via structures.

V. RESULTS AND DISCUSSIONS

The equivalent circuit model for the top layer structure was implemented in ADS software as shown in

TABLE III. RLC Values of Actual Equivalent Circuit Model of the Complete Structure

	Figure	Values
Resistance (R_1, \dots, R_{12})	10	0.015Ω
Inductance ($L_1, \dots, L_4, L_9, \dots, L_{12}$)	10	3.095pH
Inductance (L_5, \dots, L_8)	10	5.378pH
Capacitance C_{pad} ($C_1, C_3, C_4, C_5, C_7, C_8, C_{13}, C_{15}, C_{16}, C_{17}, C_{19}, C_{20}, C_{45}, \dots, C_{48}$) (top and bottom layers)	10	0.2124pF
Capacitance C_{via} ($C_2, C_6, C_{14}, C_{18}, C_{33}, \dots, C_{36}, C_{41}, \dots, C_{44}$) (top and bottom layers)	10	24.64fF
Capacitance C_{ip} ($C_9, \dots, C_{12}, C_{37}, \dots, C_{40}$) (top and bottom layers)	10	58.64pF
Capacitance C_{via} ($C_{21}, \dots, C_{24}, C_{29}, \dots, C_{32}$) (intermediate layer)	10	32.3pF
Capacitance C_{ip} (C_{25}, \dots, C_{28}) (intermediate layer)	10	44.72pF
SCLIN	10	$W = 0.255\text{mm}$ $S = 0.265\text{mm}$ $L = 50\text{mm}$ $Z = 50\Omega$
Term (1, 2, 3, 4)	10	

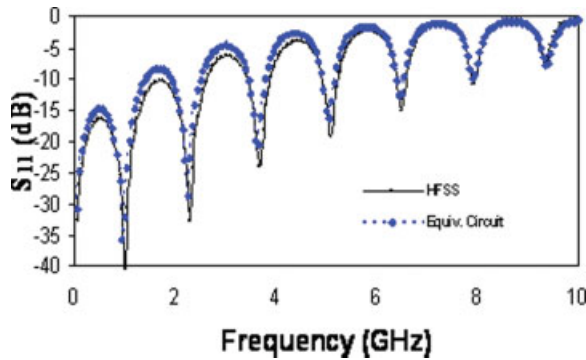


Figure 11. HFSS versus equivalent circuit simulation S_{11} parameter for the complete structure. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

Figure 7, with parameter values depicted in Table II. The reflection coefficient (S_{11}) and insertion loss (S_{21}) parameters, obtained from the simulation of the above circuit in ADS, are compared with the (S_{11}) and (S_{21}) parameters, of the top structure 3-D model, obtained from HFSS, as shown in Figures 8 and 9, respectively.

The equivalent circuits for the intermediate and bottom layer structures were also implemented and analyzed using ADS. The results from ADS were all in a good agreement with the results obtained from HFSS. Finally, the equivalent circuit for the complete structure was obtained by cascading the three equivalent circuits, from the top to the bottom layer, as shown in Figure 10, with parameter values depicted in Table III. The comparisons results of the (S_{11}) and S_{21} parameters from the ADS equivalent circuit simulation and the 3-D model from HFSS for the com-

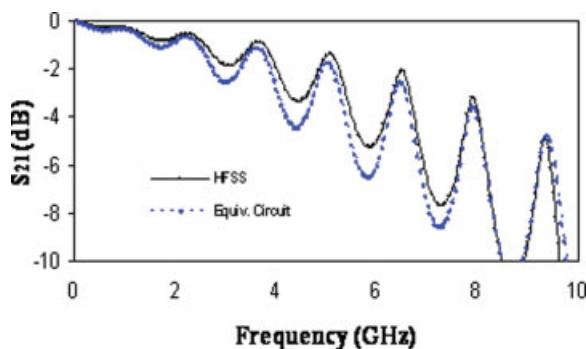


Figure 12. HFSS versus equivalent circuit simulation S_{21} parameter for the complete structure. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

plete structure are shown in Figures 11 and 12, respectively.

It can be seen from Figures 8, 9, 11, and 12, that there is a very good agreement between the HFSS differential via model and the circuit extraction method, which validates our proposed technique for characterizing differential vias. These results also agree with measurements from the same via structure reported in [1, 4].

VI. CONCLUSIONS

The purpose of this article was to characterize a differential via hole using an equivalent circuit extraction technique. The extraction technique was then used to develop an equivalent circuit model for the entire structure, which was validated by comparing the results of HFSS with the equivalent circuit simulation. Overall, the results of the scattering parameters S_{11} and S_{21} for the complete equivalent circuit, and the 3-D model simulation were very close. One of the advantages of the extraction technique is to obtain a circuit model that characterizes the differential via, which in turn, reduces the large amounts of simulation time on a very complex structure. The results shown in this article illustrate that the equivalent circuit of a complete structure model matches with a 3-D HFSS results, thus it is suitable for quickly predicting the response of the output signal of the differential via holes. Simulation time in ADS was less than a minute significantly faster than using a full wave solver. Further research includes modeling more complex middle layers and in-homogenous dielectric.

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BIOGRAPHIES



Tao Van Nguyen was born in Saigon, Vietnam. He received his Bachelor of Science degree with a major in Electrical Engineering Technology and his Master of Engineering in Electrical Engineering degree from Pennsylvania State University at Harrisburg in 1991 and 2005, respectively. He worked for AMP Incorporated as a Development Engineer for high-speed cable assemblies. Currently, he is working as an electrical engineer for Inclinator of America located in Harrisburg, Pennsylvania. His major responsibility is to develop and to design functional specifications for the electronic control of residential elevator products.



Aldo W. Morales was born in Tacna, Peru. He received his electronic engineering degree with distinction from the University of Tarapaca, Arica, Chile (formerly Northern University) and the M.S. and Ph.D. degrees in electrical and computer engineering from the State University of New York at Buffalo. From September 1990 to July 2001, he was with the College of Engineering, Penn State DuBois. He is now Associate Professor of Electrical Engineering at Penn State Harrisburg. His research interests are in mathematical morphology, digital image processing, computer vision, and neural networks. Dr. Morales was honored by the Institute of Electrical and Electronic

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Sedig S. Agili received his B.S., M.S., and Ph.D. in Electrical and Computer Engineering from Marquette University in 1986, 1989, and 1996, respectively. As a student, he was awarded fellowships from Marquette University and the U.S. Department of Education. Upon receiving his Ph.D., he joined the faculty at Marquette University where he taught several courses in electrical engineering and conducted research in the area of electro-optic devices, fiber optic communication, and fiber optic sensors. In fall of 2001, he joined the electrical engineering and electrical engineering technology programs at Penn State University, Capital College. Currently, he is teaching and conducting research in electronic communications, fiber optic communications, fiber optic sensors, and signal integrity of high-speed interconnects. He has authored numerous articles published in journals and conference proceedings, and made presentations at many conferences and seminars. He also worked for Astronaut Corporation of America in Milwaukee, Wisconsin, where he was involved in designing optical projection and heads-up display systems. He is a member of the Institute of Electrical and Electronic Engineers, American Society for Engineering Education, and Sigma Xi.